Organic Electronics 13 (2012) 18–22

Contents lists available at SciVerse ScienceDirect

Organic Electronics

journal homepage: www.elsevier.com/locate/orgel

Performance comparison of pentacene organic field-effect transistors with SiO_2 modified with octyltrichlorosilane or octadecyltrichlorosilane

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ARTICLE INFO

Article history:
Received 16 June 2011
Received in revised form 2 September 2011
Accepted 11 September 2011
Available online 18 October 2011

Keywords:
Organic field-effect transistors (OFETs)
Pentacene
Mobility
Surface treatment

ABSTRACT

Performance of pentacene organic field-effect transistors (OFETs) is significantly improved by treatment of SiO_2 with octyltrichlorosilane (OTS-8) compared to octadecyltrichlorosilane (OTS-18). The average hole mobility in these OFETs is increased from 0.4 to 0.8 cm^2/Vs when treating the dielectric with OTS-8 versus OTS-18 treated devices. The atomic force microscope (AFM) images show that the OTS-8 treated surface produces much larger grains of pentacene (~500 nm) compared to OTS-18 (~100 nm). X-ray diffraction (XRD) results confirmed that the pentacene on OTS-8 is more crystalline compared to the pentacene on OTS-18, resulting in higher hole mobility.

1. Introduction

Organic field-effect transistors (OFETs) are studied extensively because of their potential use in low-cost organic electronic applications such as smart pixels [1], radio-frequency identification tags [2], drivers for electronic paper [3], and driving circuits for flat-panel displays [4]. Pentacene is one of the most widely studied organic semiconductors for p-channel OFETs [5–9] and there have been various efforts to improve the device performance through the control of interfaces, especially the interface between the semiconductor and the gate dielectric. Treating the SiO_2 dielectric surface with self-assembled layers is one of the commonly used approaches to improve the dielectric semiconductor interface in these devices. Octadecyltrichlorosilane (OTS-18) has been used in many reports to treat SiO_2 to improve the dielectric surface properties [10–14], and to minimize the carrier trapping at the surface by passivating the hydroxyl bonds on the surface. Octyltrichlorosilane (OTS-8) is a similar silane with a shorter carbon chain, but it is a less common choice by researchers [15,16]. Both of these silanes have been referred to as OTS in many reports. Here, to avoid any confusion, we are denoting them as OTS-18 and OTS-8, where the numerals refer to the number of carbon atoms in the alkyl chain of these silane molecules. Although, many reports in the literature compare the electrical performance of pentacene OFETs and pentacene morphology upon surface treatments and modifications [12,17–19], there is no report that compares directly the performance of OFETs with SiO_2 dielectric treatment of OTS-18 and OTS-8.

Here, we report on the performance improvement in pentacene OFETs upon OTS-8 treatment of the SiO_2 gate dielectric. Several devices with varying channel lengths (L) (25–200 μm) were used for this study. The hole mobility (μ) in devices treated with OTS-8 was found to be twice that measured in devices with OTS-18. Atomic force microscope (AFM) experiments reveal that there is a significant increase in the pentacene grain sizes in OTS-8 treated devices (~500 nm) compared with devices with OTS-18. X-ray Diffraction (XRD) experiments show that the films deposited on OTS-8 with the larger grains have also a larger degree of crystallinity, which explains the larger charge mobility measured in OFETs with OTS-8. We also investigated the stability of these devices under multiple transfer characteristics scans and under continuous electrical bias stress, as well as in stress and rest conditions.

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doi:10.1016/j.orgel.2011.09.017

2. Device fabrication and electrical characterization

OFETs were fabricated on heavily doped n-type (n^+) silicon substrates (serving as the gate electrode with resistivity <0.005 Ωcm) with a 200 nm-thick thermally grown SiO_2 as the gate dielectric in a top-contact configuration. The device structure and the chemical structures of pentacene, OTS-8, and OTS-18 are shown in Fig. 1. First, the SiO_2 layer on the backside of the wafer was etched with 6:1 buffered oxide etchant, while protecting the top side with a photoresist layer. Ti/Au (10/100 nm) metallization on the backside of the substrate provided the gate electrode. The substrates were then cleaned with acetone, deionized water and isopropyl alcohol followed by O_2 plasma treatment for 2 min to make the SiO_2 surface hydrophilic. Surface treatment with OTS-8 and OTS-18 (5 mM in toluene) was performed on separate substrates by soaking them in the different OTS solutions overnight (17 h) in a N_2-filled glove box. The substrates were then rinsed with toluene and annealed at 60 °C for 5 min. The total capacitance density (C_i) was measured from the slope of a capacitance versus area plot of 12 parallel-plate capacitors on a single substrate and was found to be 16.1 nF/cm^2 for both types of substrates for this experiment. Pentacene (Sigma–Alrich) was purified using thermal gradient zone sublimation and deposited on the substrates by vacuum evaporation without any intentional substrate heating into a 50 nm-thick film. Finally, source and drain electrodes were defined by depositing a 70 nm-thick layer of Au through a shadow mask. After treatment with OTS the devices were stored in inert atmosphere and transferred in an airtight vessel into another N_2-filled glove box (O_2, H_2O < 0.1 ppm) for electrical characterization, without any exposure to atmospheric conditions. The electrical characterization was performed using an Agilent E5272A source/monitor unit. Output characteristics (drain-source current (I_{DS}) vs. drain-source voltage (V_{DS})) and transfer characteristics (I_{DS} vs. gate-source voltage (V_{GS})) were measured, and the charge mobility (μ) and threshold voltage (V_{TH}) were extracted in the saturation regime from the highest slope of $|I_{DS}|^{1/2}$ vs. V_{GS} plots using the standard saturation region current equation for thin-film transistors. For the study of stability under a constant bias, the time-dependent decay of I_{DS} was measured in the saturation regime ($V_{GS} = V_{DS} = -30$ V) for 1 h. To study the recovery between various stress cycles, I_{DS} was measured while stressing the devices for 30 min ($V_{GS} = V_{DS} = -30$ V) followed by a rest period of 20 min($V_{GS} = V_{DS} = 0$ V).

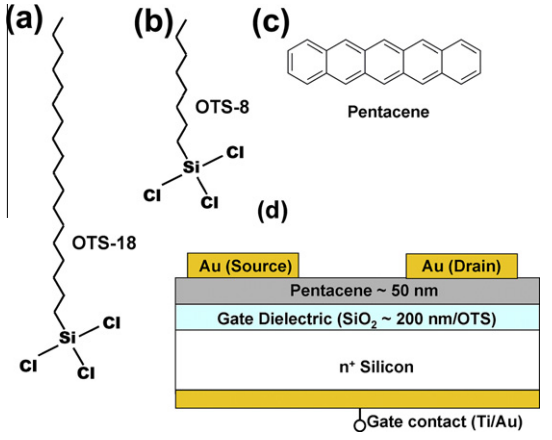

Fig. 1. Chemical structures of OTS-18 (a), OTS-8 (b), and pentacene (c); Device structure of a top-contact pentacene OFETs (d).

3. Results and discussions

OFETs with SiO_2 surfaces treated with either OTS-18 or OTS-8 with channel width of $W = 1200$ μm and various channel lengths ($L = 25$, 50, 100, and 200 μm) were characterized to obtain values of the hole mobility in the saturation regime (μ), V_{TH}, and current on/off ratios (I_{on}/I_{off}). The value of the shortest channel length was limited by the resolution of the shadow masking process. For each type of treatments, sixteen devices were characterized on each substrate with four devices for each channel length. Fig. 2a and b show the output and transfer characteristics of a device treated with OTS-18 ($W/L = 1200$ μm/100 μm), whereas Fig. 2c and d show the same for an OTS-8 treated device with same channel dimensions. As can be seen from

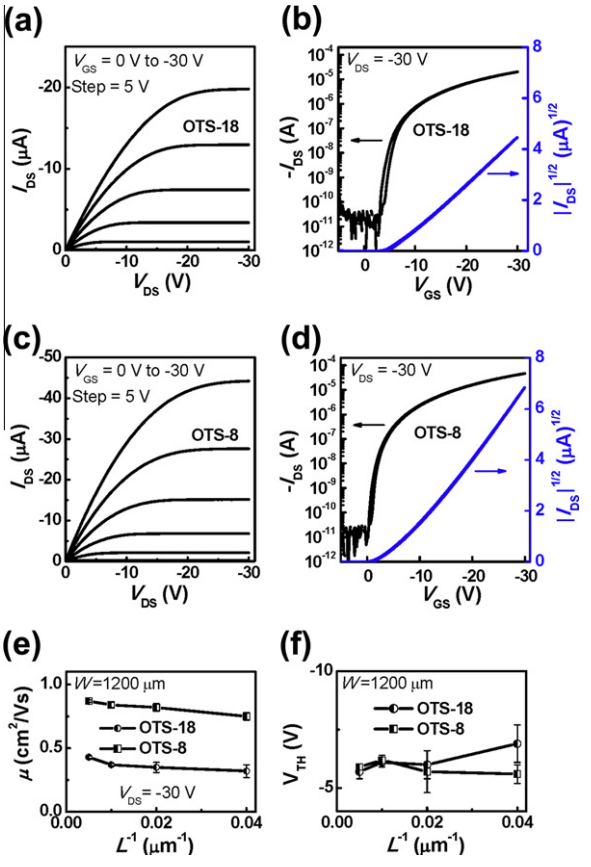

Fig. 2. Output and transfer characteristics of pentacene OFETs where SiO_2 was treated with OTS-18 (a and b), and with OTS-8 (c and d) with $W/L = 1200/100$ μm; (e) Dependence of μ of pentacene OFETs with OTS-18 and OTS-8 vs. inverse channel length (L^{-1}); and (f) threshold voltage V_{TH} vs. inverse channel length (L^{-1}) for both types of OFETs.

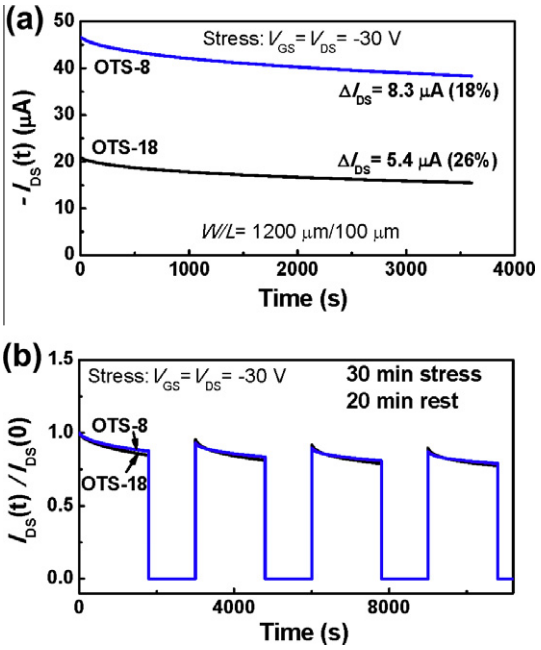

Fig. 3. (a) Decay of drain-source current (I_{DS}) for $V_{GS} = V_{DS} = -30$ V measured continuously over a period of one hour; (b) Decay of drain-source current under bias stress ($V_{GS} = V_{DS} = -30$ V) and rest ($V_{GS} = V_{DS} = 0$ V) conditions. Each stress and rest cycle consists of a 30 min stress followed by a 20 min rest period.

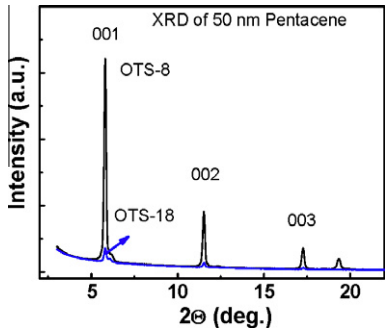

Fig. 5. XRD spectra of 50 nm-thick pentacene layers deposited on Si/SiO_2 substrates modified with OTS-8 or OTS-18.

the results, both types of devices exhibit transfer characteristics following the square law, however, there is more than a 100% increase in I_{DS} in the OTS-8 treated devices. The average μ for OFETs with OTS-18 with W/L = 1200/100 μm was 0.37 ± 0.01 cm^2/Vs, whereas the average μ for OFETs with OTS-8 was 0.84 ± 0.02 cm^2/Vs averaged over four devices with identical channel dimensions. The average V_{TH} for OTS-18 and OTS-8 devices for W/L = 1200/100 μm was -6.1 ± 0.2 and -6.2 ± 0.2 V, respectively. The plots in Fig. 2e and f show a comparison of the average μ and V_{TH} as a function of channel length (L = 25, 50, 100, and 200 μm) for both types of devices. The value of V_{TH} is nearly identical in all devices, except in devices with the shorter channel length (25 μm). The small decrease in charge mobility with decreasing channel length observed

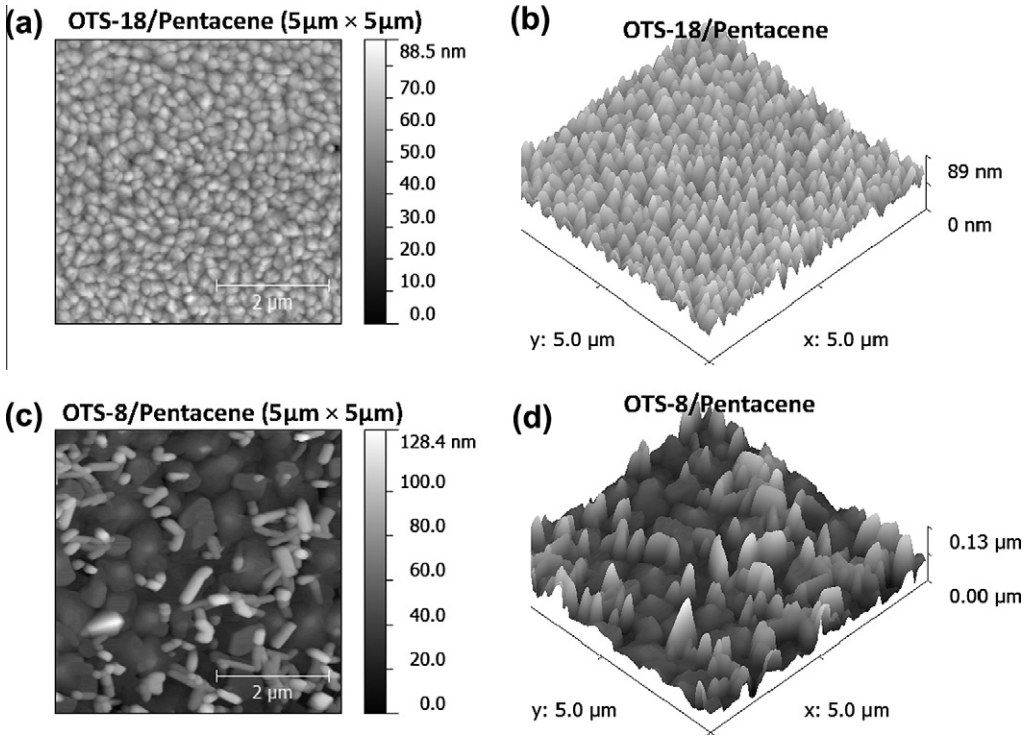

Fig. 4. AFM images of pentacene for pentacene films grown on Si/SiO_2 modified with OTS-18 (a and b) and with OTS-8 (c and d).

Table 1
Summary of results for bottom gate bottom contact (BGTC), or bottom gate top contact (BGTC) pentacene transistors on OTS-18 or OTS-8 treated SiO_2. PT is the pentacene thickness, TS is the substrate temperature, and V_{DD} is the operating voltage. Our results in this table are reported for devices with W/L of 1200/100 μm. NA: Not given/applied.

Reference	Device	OTS type	P_T (nm)	T_S (°C)	V_{DD} (V)	μ (cm^2/Vs)	V_{TH} (V)	$I_{on/off}$
Lin et al. [13]	BGTC	OTS-18	50	60	−100	0.4	+ve	1×10^8
Jackson et al. [14]	BGBC	OTS-18	30 + 20	90 and 27	−80	1.5 (max)	−8	1×10^6
Shtein et al. [10]	BGTC	OTS-18	100	40	−40	0.6–1.6	NA	$>1 \times 10^6$
Shankar et al. [12]	BGTC	OTS-18	45	70	−100	1.6 (max)	NA	NA
Virkar et al [19]	BGTC	OTS-18	45	60	−100	2.1	−27	1×10^6
Cahayadi et al. [15]	BGTC	OTS-8	50	100	−20	0.17 (ave.)	−5	8×10^5
This work, 2011	BGTC	OTS-18	50	No heating	−30	0.37 (±0.01)	−6.1(±0.2)	1×10^6
This work, 2011	BGTC	OTS-8	50	No heating	−30	0.84 (±0.02)	−6.2(± 0.2)	2×10^6

in both types of devices is due to contact resistance. High $I_{on/off}$ values in the range 10^6–10^7 are observed in both types of devices.

Fig. 3a shows the time-dependent decay of I_{DS} under a continuous DC bias stress with $V_{GS} = V_{DS} = -30$ V measured over a period of 1 h for representative devices with OTS-18 and OTS-8 with geometry W/L = 1200/100 μm. A decay of 26% and 18% from the initial value of I_{DS} is observed in OTS-18 and OTS-8 treated devices, respectively. Fig. 3b shows the comparison of the decay in I_{DS} for OTS-18 and OTS-8 samples upon bias-stress and rest tests where the devices were stressed at $V_{GS} = V_{DS} = -30$ V for 30 min followed by 20 min rest at $V_{GS} = V_{DS} = 0$ V between stress cycles. The results show that there is a small recovery in I_{DS} after rest periods, but repeated stress cycles lead to an overall decay in current.

Fig. 4 shows the AFM images of the pentacene films deposited on substrates treated with OTS-18 (Fig. 4a and b) and OTS-8 (Fig. 4c and d). The AFM images of Si/SiO_2 substrates treated with OTS-8 and OTS-18 prior to pentacene deposition looked identical and showed no differences in terms of morphology. Fig. 4c clearly shows that films of pentacene grown on substrates modified with OTS-8 exhibit larger grains compared to the pentacene on OTS-18. X-ray diffraction (XRD) experiments were performed to study the crystallinity of these films. Fig. 5 compares the XRD patterns measured in 50 nm-thick pentacene layers grown on Si/SiO_2 modified with OTS-8 and OTS-18. The pentacene film on OTS-8 shows one-order of magnitude higher XRD peaks compared to pentacene on OTS-18. The spectra measured in films grown on OTS-8 exhibit a series of (00 k) lines, identical to those reported previously by Cahyadi et al. [15] and are indicative of a higher level of crystallinity, which in turn can explain the higher mobility values measured in OFETs. Table 1 summarizes the mobility values measured in pentacene-based transistors using SiO_2 treated with OTS-18 or OTS-8 that have been reported in the literature. Unlike in our studies, the highest mobility values were found previously in devices using SiO_2 treated with OTS-18. However, a difference between previous studies and our work is the intentional heating of the substrate during deposition of the pentacene. In our case, no intentional heating of the substrate was carried out during deposition. The differences in processing conditions can explain the observed differences in performance when comparing surface modification with OTS-18 or OTS-8.

4. Summary and conclusion

In summary, p-channel pentacene OFETs were fabricated on Si/SiO_2 substrates modified with OTS-18 or OTS-8, and their electrical performance was compared. The results show that the hole mobility is improved from 0.4 to 0.8 cm^2/Vs when treating the dielectric with OTS-8 compared with OTS-18. Values of the current on-off ratios, of the threshold voltage, and electrical stability under continuous bias stress were found to be very similar. The increase in mobility observed in devices treated with OTS-8 can be attributed to larger grain sizes as measured by AFM, and to a higher degree of crystallinity as measured by XRD.

Acknowledgements

This material is based upon work supported in part by the STC Program of the National Science Foundation under Agreement No. DMR-0120967, and by the Office of Naval Research (Grant No. N00014-04-1-0120). This work was performed in part at the Microelectronics Research Center at Georgia Institute of Technology, a member of the National Nanotechnology Infrastructure Network, which is supported by NSF (Grant No. ECS- 03-35765).

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